

MITSUBISHI LSTTLs M74LS375P

4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS375P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Q and \bar{Q} .

FEATURES

- Enable inputs common to two circuits each
- Q and \bar{Q} outputs
- pin 8 GND, pin 16 V_{CC}
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and \bar{Q} . When the D signal changes, the signal that appears in outputs Q and \bar{Q} also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and \bar{Q} does not change even if D is changed.

This IC has the same functions and electrical characteristics as M74LS75P and differs only in its pin configuration.

FUNCTION TABLE (Note 1)

E	D	Q	\bar{Q}
H	H	H	L
H	L	L	H
L	X	Q^0	\bar{Q}^0

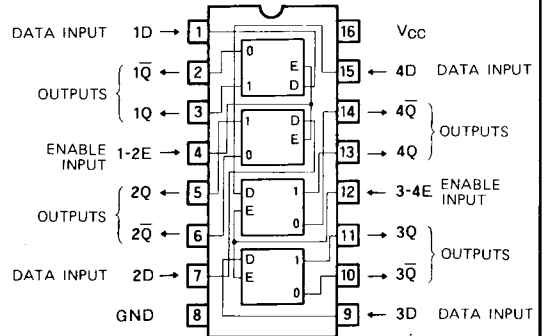
Note 1 Q^0, \bar{Q}^0 : Level of Q and \bar{Q} before the indicated steady-state input conditions were established.

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

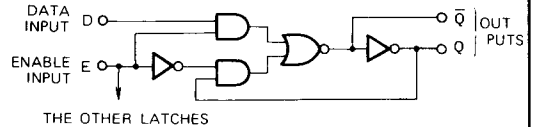
Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		-0.5 ~ +7	V
V_I	Input voltage		-0.5 ~ +15	V
V_O	Output voltage	High-level state	-0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		-20 ~ +75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65 ~ +150	$^\circ\text{C}$

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM (EACH LATCH)



4-BIT BISTABLE LATCH

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geq 2.7\text{V}$	0	-400	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0	4	mA
		$V_{OL} \leq 0.5\text{V}$	0	8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ *	Max		
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IC}	Input clamp voltage				-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = 4.75\text{V}$, $I_{IC} = -18\text{mA}$ $V_{CC} = 4.75\text{V}$, $V_I = 0.8\text{V}$ $V_I = 2\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	3.5		V	
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{V}$			0.25	0.4	V
		$V_I = 0.8\text{V}$, $V_I = 2\text{V}$			0.35	0.5	V
I_{IH}	High-level input current	D	$V_{CC} = 5.25\text{V}$			20	μA
		E	$V_I = 2.7\text{V}$			8	μA
		D	$V_{CC} = 5.25\text{V}$			0.1	mA
		E	$V_I = 10\text{V}$			0.4	mA
I_{IL}	Low-level input current	D	$V_{CC} = 5.25\text{V}$			-0.4	mA
		E	$V_I = 0.4\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-20		-100	mA	
I_{CC}	Supply current	$V_{CC} = 5.25\text{V}$ (Note 3)		6.3	12	mA	

* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

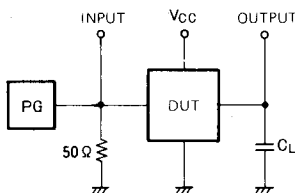
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q	$C_L = 15\text{pF}$ (Note 4)		12	27	ns
t_{PHL}			8	17	ns	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output \bar{Q}			10	20	ns
t_{PHL}			6	15	ns	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output Q			13	27	ns
t_{PHL}			12	25	ns	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output \bar{Q}			12	30	ns
t_{PHL}			6	15	ns	

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$, $t_w = 500\text{ns}$,
 $V_p = 3V_{p-p}$, $Z_0 = 50\Omega$.

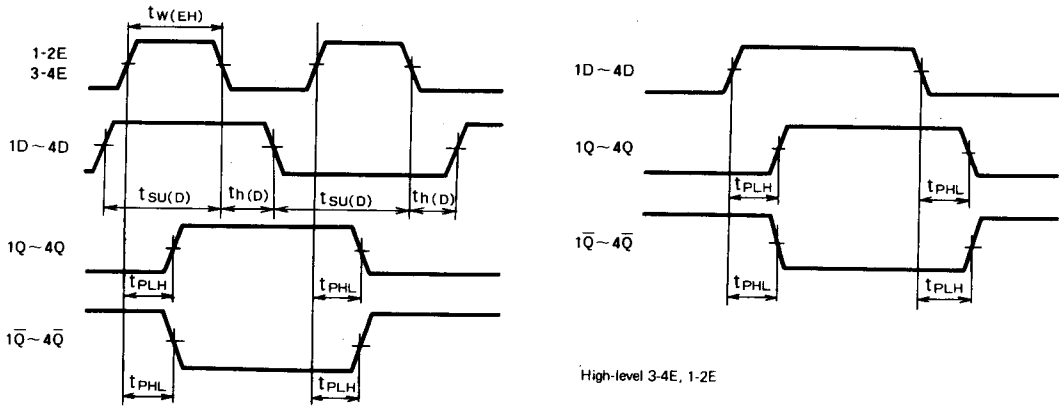
(2) C_L includes probe and jig capacitance.

4-BIT BISTABLE LATCH

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(EH)$	Enable input E high pulse width		20	7		ns
$t_{su}(D)$	Setup time 1D~4D to E		20	12		ns
$t_h(D)$	Hold time 1D~4D to E		8	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

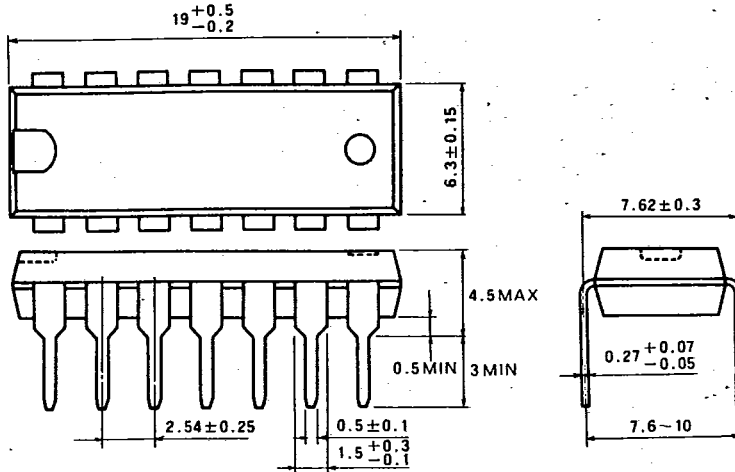


High-level 3-4E, 1-2E

T-90-20

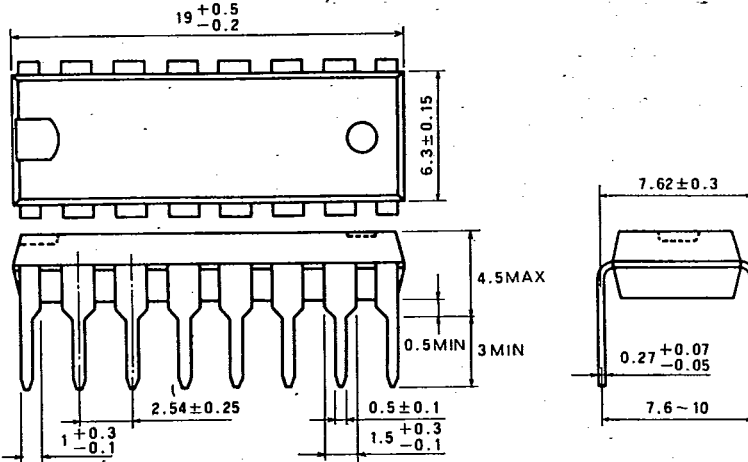
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

